

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: <b>DeWitt Jr. et al.</b>	§
	§ Group Art Unit: <b>2193</b>
Serial No.: <b>10/675,776</b>	§
	§ Examiner: <b>Vu, Tuan A.</b>
Filed: <b>September 30, 2003</b>	§
	§ Confirmation No.: <b>6262</b>
For: <b>Method and Apparatus for</b>	§
<b>Counting Execution of Specific</b>	§
<b>Instructions and Accesses to Specific</b>	§
<b>Data Locations</b>	

**35525**

PATENT TRADEMARK OFFICE  
CUSTOMER NUMBER

**Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450**

**APPEAL BRIEF (37 C.F.R. 41.37)**

This brief is in furtherance of the Notice of Appeal, filed in this case on September 15, 2010.

No fees are believed necessary, as the fee required for filing an Appeal Brief was paid on September 30, 2009, after which, prosecution was reopened by the Examiner. No additional fees are believed to be necessary. If, however, any additional fees are required, I authorize the Commissioner to charge these fees which may be required to IBM Corporation Deposit Account No. 09-0447.

### **REAL PARTY IN INTEREST**

The real party in interest in this appeal is the following party: International Business Machines Corporation of Armonk, New York.

### **RELATED APPEALS AND INTERFERENCES**

This appeal has no related proceedings or interferences.

## **STATUS OF CLAIMS**

### **A. TOTAL NUMBER OF CLAIMS IN APPLICATION**

The claims in the application are: 1-53.

### **B. STATUS OF ALL THE CLAIMS IN APPLICATION**

Claims canceled: 2-5, 7-25, 27-28, 31, 33, 36-37, and 40-53.

Claims withdrawn from consideration but not canceled: None.

Claims pending: 1, 6, 26, 29-30, 32, 34-35, and 38-39.

Claims allowed: None.

Claims rejected: 1, 6, 26, 29-30, 32, 34-35, and 38-39.

Claims objected to: None.

### **C. CLAIMS ON APPEAL**

The claims on appeal are: 1, 6, 26, 29-30, 32, 34-35, and 38-39.

### **STATUS OF AMENDMENTS**

No amendments have been filed subsequent to the previous response to office action of September 14, 2010. Therefore, the status of the claims is as presented in the response filed September 14, 2010.

## **SUMMARY OF CLAIMED SUBJECT MATTER**

### **A. CLAIM 1 - INDEPENDENT**

The subject matter of claim 1 is directed to a computer implemented method in an instruction cache of a data processing system for monitoring execution of instructions. The method comprises receiving a bundle at an instruction cache unit (Fig. 3; specification, page 23, paragraph 1), the bundle containing at least one instruction slot, (page 26, paragraph 2, FIG. 5, reference numeral 502, 504, 506) wherein the instruction slot contains an instruction (page 27, paragraph 1); responsive to receiving the bundle, determining by the instruction cache unit whether the bundle contains an indicator within at least one spare bit of the at least one instruction slot (page 27, paragraph 1), wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit (page 29, paragraph 1); responsive to a determination that the bundle contains the indicator within the at least one instruction slot, sending a signal by the instruction cache unit to a performance monitor unit (page 29, paragraph 1), wherein upon receiving the signal, the performance monitor unit increments a counter in the instruction cache unit that is associated with the instruction (page 31, paragraph 4), the incrementing providing a count of a number of times the instruction is executed (page 23, paragraph 2; page 43, paragraph 2; page 46, paragraph 1); and sending the bundle from the instruction cache unit to a functional unit for execution of the instruction (page 31, paragraph 4).

### **B. CLAIM 32 - INDEPENDENT**

The subject matter of claim 32 is directed to a computer program product that comprises a computer recordable medium having computer useable program code for monitoring execution of instructions (page 64, paragraph 1), the computer program product comprises computer usable program code (page 64, paragraph 1) for receiving a bundle at an instruction cache unit (Fig. 3; specification, page 23, paragraph 1), the bundle containing at least one instruction slot (page 26, paragraph 2, FIG. 5, reference numeral 502, 504, 506), wherein the instruction slot contains an instruction (page 27, paragraph 1); computer usable program code (page 64, paragraph 1) for, responsive to receiving the bundle, determining by the instruction cache unit whether the bundle contains an indicator within at least one spare bit of the at least one instruction slot (page 27,

paragraph 1), wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit (page 29, paragraph 1); computer usable program code (page 64, paragraph 1) for, responsive to a determination that the bundle contains the indicator within the at least one instruction slot, sending a signal by the instruction cache unit to a performance monitor unit (page 29, paragraph 1), wherein upon receiving the signal, the performance monitor unit increments a counter in the instruction cache unit that is associated with the instruction (page 31, paragraph 4), wherein the incrementing provides a count of a number of times the instruction is executed (page 23, paragraph 2; page 46, paragraph 1); and computer usable program code (page 64, paragraph 1) for, sending the bundle from the instruction cache unit to a functional unit for execution of the instruction (page 31, paragraph 4).

## **GROUND OF REJECTION TO BE REVIEWED ON APPEAL**

The grounds of rejection to review on appeal are as follows:

### **A. GROUND OF REJECTION 1**

Whether the Examiner's requirement for the Applicants to include additional limitations in the claims is improper when it is not based on any cited rule, or prior art.

## ARGUMENT

### A. GROUND OF REJECTION 1 (Claims 1 and 32)

The Examiner has indicated claims 1 and 32 allowable, but requires the Applicants to include additional limitations in the claims.

With regard to claims 1 and 32, the Examiner states the following:

Claims 1, 32 stand rejected in the Double patenting Rejection as set forth above; yet contain allowable subject matter in view of the teachings provided via Fig. 31 of the Specifications; but would be allowable if rewritten in a form including or reasonably conveying functionality of all of the constituents (see Note below) of the 'instruction cache unit' described in the pertinent section. The allowable subject matter revolves around the following scenario, pending the inclusion of *range registers, counter increment based on range execution* of Figure 31:

A instruction cache unit (ICU) having a counter therein that is incremented responsive to this ICU receiving of a spare bit and an instruction, the spare bit as an indicator to be determined by the ICU as to whether the instruction to be one to be monitored by a performance monitor unit, wherein upon receiving a signal from the ICU in response to the determination, the performance unit increments a counter implemented inside the ICU in conjunction with sending by the ICU of the instruction to a functional unit.

Note: the constituents of the ICU depicted in **Figure 31**, deemed allowable based on the previously considered Appeal Brief (per 913012009), based on the emphasis expressed therein by the arguments regarding the Inventor's particular way of implementing an "instruction cache unit" being distinguishable over any conventional instruction cache, include (see Specifications):

In this example, program 3100 includes instruction range 3102 and 3104. Each of these ranges has been identified as ones of interest for monitoring. Each of these ranges is set within an instruction unit, such as instruction cache unit 214 in FIG. 2. Each range is used to tell the processor the number of instructions executed in a range, as well as the number of times a range is entered during execution of program 3100.

Instruction cache unit 3106 uses range registers 3108 to define instruction ranges. These registers may be existing registers or instruction cache unit 3106 may be modified to include registers to define instruction ranges. These ranges may be based on addresses of instructions. Additionally, range registers 3108 may be updated by various debugger programs and performance tools.

If an instruction is executed in a range, such as instruction range 3102 or instruction range 3104, a counter is incremented in instruction cache unit 3106.

Final Office Action dated June 15, 2010, pages 5-6.

Applicants have submitted terminal disclaimers, thus overcoming the Examiner's Double Patenting Rejection.

However, the Applicants respectfully submit that the Examiner's requirement that the Applicants rewrite the claims is improper. The Examiner has not cited any Rule, Law or Prior Art that would necessitate amendments to the claims. Instead, the Examiner's attempt to require additional limitations amounts to an improper limitation on the scope of the claims.

The Examiner's requirement to rewrite the claims appears to be based on the claim not reciting additional limitations alone. In other words, the sole basis for the rejection appears to be that the claim is broad. However, "[b]readth of a claim is not to be equated with indefiniteness. *In re Miller*, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the invention to be of a scope different from that defined in the claims, then the claims comply with 35 U.S.C. 112, second paragraph". See MPEP § 2173.04. While the Examiner has not made a formal rejection of the claims under 35 U.S.C. 112, second paragraph, the Examiner's requirement to rewrite the claims substantively identical to a rejection under 35 U.S.C. 112, second paragraph. Definiteness under 35 U.S.C. 112, second paragraph does not require the Applicants to enumerate every possible claim feature. No such requirement exists in the MPEP, nor anywhere else under U.S. patent law.

Because the Examiner has not cited anything that would necessitate amendments to the claims, and the Examiner has not made any rejection to the claims under any Rule, the Examiner's requirement that the Applicants rewrite the claims is improper and should be withdrawn.

**C. CONCLUSION**

As shown above, the Examiner has failed to state valid rejections against any of the claims. Therefore, Applicants request that the Board of Patent Appeals and Interferences reverse the rejections. Additionally, Applicants request that the Board direct the Examiner to allow the claims.

Date: December 1, 2010

Respectfully submitted,

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## **CLAIMS APPENDIX**

The text of the claims involved in the appeal is as follows:

1. A computer implemented method in an instruction cache of a data processing system for monitoring execution of instructions, the method comprising:

receiving a bundle at an instruction cache unit, the bundle containing at least one instruction slot, wherein the instruction slot contains an instruction;

responsive to receiving the bundle, determining by the instruction cache unit whether the bundle contains an indicator within at least one spare bit of the at least one instruction slot, wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit;

responsive to a determination that the bundle contains the indicator within the at least one instruction slot, sending a signal by the instruction cache unit to a performance monitor unit, wherein upon receiving the signal, the performance monitor unit increments a counter in the instruction cache unit that is associated with the instruction, the incrementing providing a count of a number of times the instruction is executed; and

sending the bundle from the instruction cache unit to a functional unit for execution of the instruction.

6. The computer implemented method of claim 1, wherein the counter is located in a shadow memory.

26. The computer implemented method of claim 1, wherein the bundle contains the indicator in a spare field of the bundle.

29. The computer implemented method of claim 1, further comprising:
- responsive to a determination that the bundle contains the indicator, incrementing the counter, wherein the counter tracks any subsequent instruction executed by an associated processor.
30. The computer implemented method of claim 29, wherein the bundle is a first bundle, the method further comprising:
- receiving a second bundle at the instruction cache;
- responsive to receiving the second bundle, determining whether a second instruction in the second bundle contains a second indicator; and
- responsive to a determination that the second bundle contains the second indicator, ending the incrementing of the counter.
32. A computer program product comprising:
- a computer recordable medium having computer useable program code for monitoring execution of instructions, the computer program product comprising:
- computer usable program code for receiving a bundle at an instruction cache unit, the bundle containing at least one instruction slot, wherein the instruction slot contains an instruction;
- computer usable program code for, responsive to receiving the bundle, determining by the instruction cache unit whether the bundle contains an indicator within at least one spare bit of the at least one instruction slot, wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit;

computer usable program code for, responsive to a determination that the bundle contains the indicator within the at least one instruction slot, sending a signal by the instruction cache unit to a performance monitor unit, wherein upon receiving the signal, the performance monitor unit increments a counter in the instruction cache unit that is associated with the instruction, wherein the incrementing provides a count of a number of times the instruction is executed; and

computer usable program code for, sending the bundle from the instruction cache unit to a functional unit for execution of the instruction.

34. The computer program product of claim 32, wherein the computer usable program code for incrementing the counter further comprises computer usable program code for incrementing the counter, wherein the counter is located in a shadow memory.

35. The computer program product of claim 32 further comprising wherein the bundle contains the indicator in a spare field of the bundle.

38. The computer program product of claim 32, further comprising:

computer usable program code, responsive to a determination that the bundle contains the indicator, incrementing the counter, wherein the counter tracks any subsequent instruction executed by an associated processor.

39. The computer program product of claim 38 wherein the bundle is a first bundle, the computer program product further comprising:

computer usable program code for receiving a second bundle at the instruction cache unit;

computer usable program code, responsive to receiving the second bundle, for determining whether a second instruction in the second bundle contains a second indicator; and

computer usable program code, responsive to a determination that the second bundle contains the second indicator, for ending incrementing the counter.

## **EVIDENCE APPENDIX**

This appeal brief presents no additional evidence.

## **RELATED PROCEEDINGS APPENDIX**

This appeal has no related proceedings.